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EXAMINER	
NATNAEL, PAULOS M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,404	HU ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-26,28-31,33-44 and 46-50* is/are rejected.

7)☒ Claim(s) *20,27,32 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-19, 21-26, 28-31,33-44,46-50** are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmes et al., U.S. Pat. No. 6,049, 769.

3.

Considering claim **1**, A method of synchronizing a digital audio signal with a corresponding digital video signal comprising:

b) setting the encoding parameters of a digital signal processor prior to receiving a start command from a host; is implied because without setting some sort of encoding procedure using predetermined parameters, the DSP would not function properly as desired.

c) receiving the start command from the host instructing the digital signal processor to begin encoding the audio frame in response to a first video synchronization signal, is also implied because the DSP is controlled by the microprocessor **48 which is in control of operations within the peripheral board 10**, and the Microprocessor would issue a start or stop command to the DSP.

d) receiving the first video synchronization signal at the digital signal processor, is met by vertical synch 142 that is received by DSP 160 from Video I/O 35, Fig.4;

e) encoding the audio frame at the audio sampling rate upon receiving the first's video synchronization signal, is met by DSP 160 which encodes the audio frame at an audio sampling rate.

Except for;

a) temporarily storing an audio frame sampled at an audio sampling rate ***in a digital signal processor (DSP) prior to encoding.***

Regarding a), Holmes et al. do not specifically discloses the audio data temporarily stored in the DSP. Holmes however disclose "the DSP also controls the flow of data from/to the ADC FIFO 176"[col. 5, lines 25-26]...Because the data are queued in ADC FIFO 176, DSP 160 can empty ADC FIFO 176 at its leisure and need not constantly monitor an input line to pick up each bit of the input serial stream.[col. 6, lines 64-67*]* The input/output ports comprise ADC and DAC converters which, in turn, include one FIFO memory each. The FIFOs store the audio signal temporarily. The DSP is a special processor designed for high speed data manipulation specially used in audio communications, image manipulation and other data acquisition and data control applications. (Microsoft Press, Computer Dictionary, 3rd edition, 1997) The DSP may include a memory device as other types of processors do. Therefore, it would have been obvious to those with ordinary skill in the art at the time the invention was made to modify

the system of Holmes et al by providing the FIFO memories within the DSP, so that the system is made compact and perhaps less costly, because the DSP would use its own memory to store audio data temporarily instead of utilizing another, separate memory device, which would make the system as a whole larger in size which in turn is not a desirable feature in electronics design.

Considering claim **2**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, further comprising transmitting a boot command from the host to the digital signal processor, is implied because the Microprocessor 48 controls the DSP 160 (fig. 4), it would send different commands including start/stop and other commands.

Considering claim **3**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 2, wherein the boot command resets a buffer of the DSP along with a controller.

See rejection of claim 2.

Considering claim **4**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 2, wherein the controller is operable to accept and transfer the audio frame and communications from and to the encoder.

See rejection of claim 1;

Considering claim 5, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 2, wherein the buffer is operable to store and transfer the audio frames, is met by FIFO 186 and 176, fig.4

Considering claim 6, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 2, wherein the boot command activates a program interface that facilitates communications between the host and the DSP, is met by the DSP DATA Bus 188, and Peripheral data bus 40, fig.4;

Considering claim 7, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 2, further comprising sending a ready signal from the DSP back to the host confirming the execution of the boot command.

See rejection of claim 2;

Considering claim 8, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim I, further comprising transmitting video synchronization signals to the audio encoder, is met by the vertical synch signal 142, fig.4;

Considering claim 9, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, further comprising communicating a plurality of encoding characteristics of the audio frame to the host.

See rejection of claim 2;

Considering claim **10**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 9, wherein the encoding characteristics reflect the frequency and bit rate of the audio frame, is met by the disclosure that "Input ADC 152 accepts analog audio input from an external audio device through audio input port 32, and samples the audio at the rate determined by the audio sampling frequency. The samples are presented in bit-serial form from ADC 152; this is converted to 16-bit parallel form by serial-to-parallel converter 174, and then reformatted into 32-bit words and queued in ADC FIFO 176. Because the data are queued in ADC FIFO 176, DSP 160 can empty ADC FIFO 176 at its leisure and need not constantly monitor an input line to pick up each bit of the input serial stream." (col. 6, lines 57-68)

Considering claim **11**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 10, wherein the bit rate of the audio frame corresponds to its rate of compression.

See rejection of claim 10.

Considering claim **12**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, further comprising sending a preparatory command to the encoder that sets a plurality of encoding parameters of the encoder according to the encoding characteristics of the audio frame.

See rejection of claim 2;

Considering claim **13**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, wherein the encoding parameters reflect characteristics of the audio frame such as frequency and bit rate.

See rejection of claim 10;

Considering claim **14**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, wherein host uses the encoding characteristics to establish new encoding parameters, use default encoding parameters or repeat the encoding parameters from a previous application, is implied because the host microprocessor would control the encoding parameters.

Considering claim **15**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, wherein the first video synchronization signal is the next generated video synchronization signal

immediately following the transmission of the start command from the host, is met by the vertical synch signal 142, fig.4.

Considering claim **16**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, further comprising transmitting a status signal back to the host when the encoding parameters of the encoder are set.

See rejection of claim 2;

Considering claim **17**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, wherein the beginning of the audio encoding process coincides with the same video synchronization signal that marks the beginning of the video encoding process, is implied in the system of Holmes that is synchronizing digital audio to digital video.

Considering claim **18**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 1, wherein the host is any suitable microprocessor, is met by the microprocessor 48, fig.4;

Considering claim 19, (Current Amended) A method of synchronizing a digital audio signal with a corresponding digital video signal comprising:
receiving a first video synchronization signal: receiving a stop command from a host instructing a digital signal processor to count the number audio samples of

the audio frame occurring subsequent to the occurrence of a second video synchronization signal; receiving a second video synchronization signal at the digital signal processor; and counting the number of samples of an audio frame representing a time duration equal to the difference between the second video synchronization signal and a last encoded sample of the audio frame.

Regarding claim 19, see rejection of claim 41.

Considering claim 21, (Original) A method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 19, wherein the counted samples contain encoding instructions, is implied because without counted samples of audio, the DSP would be unable to process the encoding process.

Considering claim **22**, (Original) A method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 19, wherein the ending of the audio encoding process coincides with the same video synchronization signal that marks the ending of the video encoding process, is implied because the audio and video signals are being synchronizing.

Considering claim **23**, (Original) a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 19, wherein the host is any suitable microprocessor, is met by host microprocessor **48**, fig.4;

Considering claim **24**, (Original) A method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 19, wherein the stop command further instruct the DSP to cease encoding process upon encoding the last sample of the audio frame.

Considering claim **25** (Original) A method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 19, further comprising transmitting the encoded audio frame to a multiplexor to be combined with a corresponding video frame.

Considering claim 26, (Original) A method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 19, further comprising transmitting video synchronization signals to the audio encoder, is met by video sync signal 142, fig.4;

Considering claim **28**, Homes discloses the following claimed subject matter, note;

a) an audio generating means for generating an audio frame at an audio sampling rate; a video generating means for generating a video frame and a plurality of video synchronization signals, is met by the disk 24, fig.3 and by the video I/O 35 (fig.4); (see col. 3, lines 38-43)

b) a digital signal processor is met by the DSP 160 which receives a vertical synch signal 142 , Fig.4;

c) a host microprocessor operable to send command signals to, and to set the encoding parameters of the digital signal processor application, is met by Host Computer 12, fig.3;

except for;

d) the claimed DSP "operable to temporarily store the audio frame, then encode the audio frame at an audio sampling rate in response to a first video synchronization signal."

Regarding d), Holmes discloses a DSP that receives a vertical synch signal 142, fig.4 and synchronizes the audio/video data according to the received vertical synch 142, which is a video clock (see fig.4), output from the Video Input/output 35, fig.4. Holmes et al specifically disclose "The audio data should also be synchronized to the video data on a frame-by-frame basis, since there may not be an integer number of audio samples for each frame of video. To handle this, synch pulse 142 of the video clock is provided from video I/O port circuit 35 to digital signal processor (DSP) 160 as a frame interrupt..." (see also col. 5, lines 15-29) The DSP is coupled to Audio input/output ports 32 and 36 (fig. 4). The input/output ports comprise ADC and DAC converters which in turn include one FIFO memory each. The FIFOs store the audio signal temporarily. The DSP is a special processor designed for high-speed data manipulation specially used in audio communications, image manipulation and other data acquisition and data control applications. (Microsoft Press, Computer Dictionary,

3rd edition, 1997) The DSP may include a memory device as other types of processors do. Therefore, it would have been obvious to those with ordinary skill in the art at the time the invention was made to modify the system of Holmes et al by providing FIFO memories within the DSP, so that the system would be made compact and thus less costly, because the DSP would use its own memory to store data instead of utilizing another, separate memory device.

Considering claim **29**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 28, wherein the digital signal processor must first receive a start command from a host prior to encoding the audio frame, is implied because the Microprocessor 48 controls the DSP 160 (fig. 4), it would send different commands including start/stop commands.

Considering claim **30**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 28, wherein the first video synchronization signal is the next generated video synchronization signal immediately following the transmission of the start command from the host.

See rejection of claim 29.

Considering claim **31**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 28, wherein the DSP comprises an encoder, a buffer and a controller.

Regarding claim 31, Holmes does not specifically disclose an encoder buffer and controller. However, the DSP of Holmes is encoding and synchronizing audio signal with video signals. (see col. 2, lines 44-50) And as shown in the rejection of claim 28 above, the DSP may comprise a memory device; and the DSP is a processor designed for high-speed data manipulation specially used in audio communications, image manipulation and other data acquisition and data control applications. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Holmes by providing the DSP with a memory device and microprocessor in order to make the system of Holmes more compact and thus efficient and less costly.

Considering claim **33**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 31, wherein the controller is operable to accept and transfer audio frames and communications from and to the encoder.

See rejection of claim 31.

Considering claim **34**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 31, wherein the buffer is operable to store and transfer audio frames.

See rejection of claim 28 (c).

Considering claim **35**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 28, wherein a plurality of video synchronization signals are generated periodically, is met by video synch 142, fig.4;

Considering claim **36**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 28, wherein the digital signal processor transmits the audio frame to the multiplexor upon encoding the audio frame.

Regarding claim 36, Holmes does not specifically disclose a multiplexor. Holmes et al use separate processing paths for the video and audio signals, and their invention "allows and facilitates the use of multiple video formats with audio separately or simultaneously recorded, and for synchronizing audio to multiple format video on playback" (col. 8, lines 55-58) Holmes et al. do not specifically disclose a multiplexor means for multiplexing the audio signal and the video signal. However, the Examiner takes Official Notice in that it is well known in the art to utilize a multiplexer to combine the different data such as the audio and video data, and therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Holmes et al by providing a multiplexer to combine the signals so that the transmission of data would be efficient.

Considering claim **37**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 28, including a programming interface present between the digital signal processor and the host to facilitate communication of a plurality of commands and status signals, is met by the DSP data bus 188, fig.4;

Considering claim **38**, a data transmission apparatus for synchronizing an audio signal with a video signal according to above claim 37, wherein the status signals include responses from the digital signal processor to host confirming the execution of the host's instructions, is implied because the DSP communicates with the microprocessor 48 through the peripheral data bus 40 as well as the DSP data bus 188, fig.4;

Considering claim **39**, a data transmission apparatus for synchronizing an audio signal with a video signal according to the claim 37, wherein the plurality of commands include communications from the host to the digital processor authorizing the execution of
processing functions, requesting status signals and setting encoding parameters.

See rejection of claim 38.

Considering claim **40**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 28, further comprising a

demultiplexor means for separating the audio signal and the video signal from a multiplexed signal in accordance with a control signal, prior to generation.

The reference of Holmes "features an audio/video input port apparatus for acquiring one or multiple channels of digital audio samples." (col. 1, lines 61-63) Holmes et al use separate processing paths for the video and audio signals, and their invention "allows and facilitates the use of multiple video formats with audio separately or simultaneously recorded, and for synchronizing audio to multiple format video on playback" (col. 8, lines 55-58) Holmes et al. do not specifically disclose a demultiplexor means for separating the audio signal and the video signal. However, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Holmes by utilizing a demultiplexor to separate the signals so that the processing is made efficient by making the system compact or less complicated.

Considering claim **41**, Shiba discloses the following claimed subject matter, note; a) an audio generating means for generating an audio frame, is met by the disk 24, fig.3 and by the video I/O 35 (fig.4); (see col. 3, lines 38-43)

b) a video generating means for generating a video frame and first and second video synchronization signals, is also met by the disk 24, fig.3 and by the video I/O 35 (fig.4); (see col. 3, lines 38-43)

c) a digital signal processor (DSP) operable to count the number of samples of an audio frame representing a time duration equal to the difference between a second video synchronization signal and a last encoded sample of the audio frame in response to receiving a stop command, is met by DSP 160, fig. 4;

c) to count the number of samples of an audio frame representing a time duration equal to the difference between the second video synchronization signal and a last encoded sample of the audio frame in response to receiving a stop command, is **implied** because Holmes disclose the DSP receiving the video synchronization signal 142 as a frame interrupt, the video sync signal occurs to synchronize the video and audio signals, and the DSP would have to take account of that repeated occurrence of the sync signal by counting or other method to track it.

d) a host microprocessor operable to generate and transmit the start command to the digital signal processor, is met by Host Computer 12, fig.3;

Except for;

e) multiplexor means for combining the encoded audio signal with the video signal, is **implied**, because audio and video outputs are combined, multiplexed, or added together for efficient transmission to another device.

Regarding e), Holmes does not disclose a multiplexer to combine the encoded video and audio signals. However, the examiner takes official notice in that such method of combining video and audio signals is notoriously well known

in the art and, thus, it would have been obvious to those with ordinary skill in the art at the time the invention was made to modify the system of Holmes et al by providing a combiner, an adder or a multiplexer to combine the signals in order to make it easier to transmit the signals together efficiently.

Considering claim **42**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 41, wherein the digital signal processor transmits to the host a value corresponding to the time required to process the counted audio frames, is implied because the DSP must communicate with the Host device in order to process the data properly.

Considering claim **43**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 41, wherein the second video synchronization signal is the next generated video synchronization signal immediately following the transmission of the stop command from the host, is also implied because the first video signal is used to synchronize the two signals.

Considering claim **44**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 41, wherein the DSP comprises an encoder, a buffer and a controller.

Regarding claim 44, Holmes et al disclose a DSP which is used for encoding the audio data and could include. Holmes et al do not specifically disclose DSP comprises a buffer. However, the Examiner takes Official Notice

here in that it is notoriously well known in the art that digital signal processors (DSP) comprise and encoder, a storage device, and a microprocessor or controller and, therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Holmes by providing a FIFO memory such as illustrated as FIFO 176 in fig.4 or a buffer in order to make the system of Holmes more compact.

Considering claim **46**, a method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 44, wherein the controller is operable to accept and transfer audio frames and communications from and to the encoder;

See rejection of claim 44;

Considering claim **47**, a method of, synchronizing a digital audio signal with a corresponding digital video signal according to claim 44, wherein the buffer is operable to Store and transfer audio frames.

See rejection of claim 44.

Considering claim **48**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 41, wherein a plurality of video synchronization signals are generated periodically, is met by video I/O 35 that generates the video sync signals. (Fig. 4)

Considering claim **49**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 41, wherein the digital signal processor transmits the audio frame to the multiplexor upon encoding the audio frame, is implied because the encoded audio/video data would be output to the next stage and would need to be multiplexed. (see also rejection of claim 41 (e)).

Considering claim **50**, a data transmission apparatus for synchronizing an audio signal with a video signal according to claim 41, including a programming interface present between the digital signal processor and the host to facilitate communication of a plurality of commands and status signals, is met by peripheral data bus 40, Fig. 2;

Response to Arguments

4. Applicant's arguments filed 8/05/2004 have been fully considered but they are not persuasive. Response follows:

Applicant's Arguments

To this end, independent claims 1 and 28 have been amended to recite an audio frame that is encoded at the same audio sampling rate at which it is received. That is, the audio sampling rate is not adjusted prior to encoding. This claimed feature is distinguishable from the apparatus disclosed in Holmes, ***which adjusts the audio sampling rate.***

Examiner's Response

Firstly, the applicant's representative is arguing something that is not found in claim 1. Claim 1 does not recite "audio frame that is encoded at the same audio sampling rate at which it is received." Rather, amended claim 1 reads "an audio generating means for generating an audio frame at an audio sampling rate". The ***audio sampling rate*** is clearly disclosed by Holmes et al.

Secondly, Holmes et al disclose that "For PAL video...no adjustment is needed..." (col. 7, lines 7-11) The argument therefore that Holmes adjusts the audio sampling rate, is unpersuasive, because for at least the PAL video signal, Holmes et al. teach that no sampling rate adjustment is needed.

Allowable Subject Matter

5. Claims **20,27,32 and 45** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose method of synchronizing a digital audio signal with a corresponding digital video signal according to claim 19, further comprising discarding the counted samples prior to combining the remaining portion of the audio frame with the video frame in anticipation of playback, as in claim **20**; a method of synchronizing a digital audio signal with a corresponding digital video signal, wherein the second video synchronization

signal is the next generated video synchronization signal immediately following the transmission of the stop command from the host, as in claim **27**;

Data transmission apparatus for synchronizing an audio signal with a video signal comprising an encoder, wherein the encoder includes a number of registers for storing data being processed, an arithmetic and logic unit for performing logical operations as well as arithmetic operations, and a parallel connected bit shifting unit for performing bit shifting and masking, as in claims **32 and 45.**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
December 30, 2004

PAULOS M. NATNAEL
PATENT EXAMINER